WHAT IS CLAIMED IS:

1. An electrostatic discharge (ESD) protection circuit comprising:

a stacked NMOS transistor pair coupled between a pad and a negative voltage supply with a first transistor's drain connected to the pad and a second transistor's source connected to the negative power supply;

a first voltage divider providing reduced voltage from a high voltage positive power supply to a gate of the first transistor;

a first diode string coupled between the gates of the first and second transistors;

a second diode string with its anode end coupled to the pad;

an inverter with a source of a PMOS transistor thereof, coupled to a cathode end of the second diode string and with its NMOS transistor coupled to the negative power supply, along with an output node of the inverter being coupled to a gate of the second transistor; and

a RC circuit coupled to an input node of the inverter,

wherein an ESD current travels through the stacked NMOS transistor pair for dissipation.

2. The circuit of claim 1 wherein the protection circuit is coupled to at least one pad that is connected to a high voltage positive power supply.

3. The circuit of claim 1 wherein all the transistors are low voltage transistors.

4. The circuit of claim 1 wherein the RC circuit, the second diode string, and the first voltage divider collectively turn on the first and second transistors in the stacked NMOS transistor pair while dissipating the ESD current.

5. The circuit of claim 1 further comprising a high voltage output driver circuit coupled thereto, wherein the ESD current initiated on an output pad of the driver circuit discharges through the stacked NMOS transistor pair.

6. The circuit of claim 5 wherein the high voltage output driver circuit uses low voltage transistors.

7. The circuit of claim 6 wherein the high voltage output driver circuit has at least two PMOS transistors and two NMOS transistors coupled in series respectively wherein a gate voltage of two transistors is adjusted so that a stress caused by the high voltage positive power supply is reduced on each transistor.

8. An electrostatic discharge (ESD) protection circuit having only low voltage transistors, the circuit comprising:

a stacked NMOS transistor pair coupled between a pad and a negative voltage supply with a first transistor's drain connected to the pad and a second transistor's source connected to the negative power supply;

a first voltage divider providing a reduced voltage from a high voltage positive power supply to a gate of the first transistor;

a first diode string coupled between the gates of the first and second transistors;

an inverter with a source of a PMOS transistor thereof coupled to the pad and

with its NMOS transistor coupled to the negative power supply, along with an output node of the inverter being coupled to a gate of the second transistor; and

a RC circuit coupled to an input node of the inverter,

wherein an ESD current travels through the stacked NMOS transistor pair for dissipation.

9. The circuit of claim 8 further comprising a second diode string with its anode end coupled to the pad, and its cathode end coupled to the inverter.

10. The circuit of claim 8 wherein the protection circuit is coupled to at least one pad that is connected to a high voltage positive power supply.

11. The circuit of claim 8 wherein the RC circuit, and the first voltage divider, collectively, turn on the first and second transistors in the stacked NMOS transistor pair while dissipating the ESD current.

12. The circuit of claim 8 further comprising a high voltage output driver circuit coupled thereto, wherein the ESD current initiated on an output pad of the driver circuit discharges through the stacked NMOS transistor pair.

13. The circuit of claim 12 wherein the high voltage output driver circuit uses low voltage transistors.

14. The circuit of claim 8 wherein the RC circuit has predetermined resistance and capacitance to assure that the inverter's output node stays high initially when the ESD current starts.

15. A circuit with high voltage power supply integrated with an electrostatic discharge (ESD) protection mechanism using low voltage transistors, the circuit comprising:

an ESD protection circuit using only low voltage transistors, the ESD protection circuit further comprising:

a stacked NMOS transistor pair coupled between a pad and a negative voltage supply with a first transistor's drain connected to the pad and a second transistor's source connected to the negative power supply;

a first voltage divider providing a reduced voltage from a high voltage positive power supply to a gate of the first transistor;

a first diode string coupled between the gates of the first and second transistors;

a second diode string with its anode end coupled to the pad;

an inverter with a source of a PMOS transistor thereof coupled to a cathode end of the second diode string and with its NMOS transistor coupled to the negative power supply, along with an output node of the inverter being coupled to a gate of the second transistor; and

a RC circuit coupled to an input node of the inverter; and

an application circuit using the high voltage power supply as its operation voltage;

wherein an ESD current initiated from the application circuit travels through the stacked NMOS transistor pair of the ESD protection circuit for dissipation.

16. The circuit of claim 15 wherein the ESD protection circuit is coupled with the application circuit through a high voltage power supply node.

17. The circuit of claim 15 wherein the RC circuit, the second diode string, and the first voltage divider, collectively, turn on the first and second transistors in the stacked NMOS transistor pair while dissipating the ESD current.

18. The circuit of claim 15 wherein the application circuit is a high voltage output driver circuit, wherein the ESD current initiated on an output pad of the driver circuit discharges through the stacked NMOS transistor pair.

19. The circuit of claim 18 wherein the high voltage output driver circuit uses low voltage transistors.

20. The circuit of claim 19 wherein the high voltage output driver circuit has at least two PMOS transistors and two NMOS transistors coupled in series, respectively, wherein a gate voltage of two transistors is adjusted so that stress caused by the high voltage positive power supply is reduced on each transistor.